REMARKS

Claims 1-2, 4, and 18-20 are pending in this application. Claims 18-20 are currently withdrawn from further consideration. By this Amendment, claims 1-2, 4, and 18-20 are amended. No new matter is added. Reconsideration in view of the above amendments and the following remarks is respectfully requested.

The courtesies extended to Applicant's representative by Examiner Sefer at the interview held August 1, 2006, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicant's record of the interview.

I. Claims Define Patentable Subject Matter

The Office Action rejects claims 1-2 and 4 under 35 U.S.C. §102(b) as being anticipated by Matsuda (Japanese Patent Document No. 11-231805); and further rejects claims 1-2 and 4 under 35 U.S.C. §103(a) as being unpatentable over Tam (U.S. Patent Application Publication No. 2002/0021293) in view of Kunii (U.S. Patent No. 5,412,493). Applicant respectfully traverses these rejections.

A. §102(b) Rejection over Matsuda

Regarding the §102(b) rejection over Matsuda, Applicant respectfully asserts that Matsuda fails to disclose a p-channel single gate driving thin-film transistor including at least the source region and the drain region including regions adjacent to the active region, the adjacent regions including lightly doped impurity regions with an impurity concentration *less than* an impurity concentration of the drain region, as recited in independent claim 1.

Matsuda, in Fig. 1, discloses two transistors 30 and 40. Transistor 40 controls the electroluminescence element 60, and transistor 30, which has a double-gate structure, operates as a switching transistor. Matsuda further discloses that the switching transistor 30 includes a source area 5 which has an impurity concentration higher than doped regions 4

bordering the active regions 3. Further, in Fig. 1, Matsuda discloses that controlling transistor 40 includes a drain 16 connected to a power supply, and a source 15 connected to the electroluminescent element 60. Further, as shown in Fig. 1, the controlling transistor 40 includes an active region 3, on either side of which are located doped regions 4. The doped region 4 on the drain side of transistor 40 appears to be longer than the doped region 4 on the source side of transistor 40.

However, Matsuda does not disclose or suggest that either the drain region 15 or the source region 16 have an impurity concentration higher than that of the doped regions 4 of transistor 40. Matsuda merely discloses that only the source area 5 of switching transistor 30 has an impurity concentration higher than the doped regions 4. Accordingly, since Matsuda does not disclose that transistor 40 is p-type; and, more importantly, does not disclose that transistor 40 includes doped impurity regions with an impurity concentration less than an impurity concentration of the drain region, Matsuda fails to disclose a p-channel single gate driving thin-film transistor including at least the source region and the drain region including regions adjacent to the active region, the adjacent regions including lightly doped impurity regions with an impurity concentration *less than* an impurity concentration of the drain region, as recited in independent claim 1.

B. §103(a) Rejection over Tam in view of Kunii

Regarding the §103(a) rejection, Applicant respectfully asserts that it would not have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tam with the teachings of Kunii to produce the p-channel single gate driving thin-film transistor including at least asymmetric lightly-doped impurity regions, as recited in claim 1, because Kunii teaches away from the combination of Tam's *single*-gate transistor and Kunii's lightly-doped region arrangement in *double*-gate transistors.

Tam, in Figs. 3 and 5, discloses a *single*-gate p-channel transistor driving an organic electroluminescent device (OELD). Kunii, in Fig. 16, discloses a *double*-gate transistor driving a picture element wherein the lightly-doped region 63 on the source/drain region side is smaller than the lightly-doped region 64 on the drain region side. The Office Action asserts that the motivation to combine Tam and Kunii is to suppress leak current, as taught by Kunii. However, Applicant respectfully asserts that Kunii teaches away from incorporating any kind of lightly-doped region structure in a *single*-gate transistor.

Specifically, Kunii, in col. 19, Table 1, states that, for a single LDD arrangement (item 8), where the arrangement includes only a *single*-gate lightly-doped drain thin film transistor with lightly-doped regions on each side of the active region, the leak current is greater than that for a *double* LDD arrangement. Moreover, Kunii, in col. 20, lines 13-17, teaches that a *single* thin-film transistor cannot suppress leak current sufficiently and the requirement that "the leak current is sufficiently low using a single thin film transistor" is not satisfied. Further, Kunii, in col. 20, lines 35-38, states that the advantages of a *multi*-gate lightly-doped drain thin-film transistor structure are very significant.

Thus, Applicant respectfully asserts that because Kunii discourages the use of lightly-doped region arrangements in *single*-gate transistors in favor of lightly-doped region arrangements in *double*-gate transistors, due to known disadvantages of such *single*-gate transistors, Kunii teaches away from the combination of Tam's *single*-gate transistor and Kunii's lightly-doped region arrangement in *double*-gate transistors. Consequently, it would not have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tam with the teachings of Kunii to produce the p-channel single gate driving thin-film transistor including at least asymmetric lightly-doped impurity regions, as recited in claim 1.

II. Conclusion

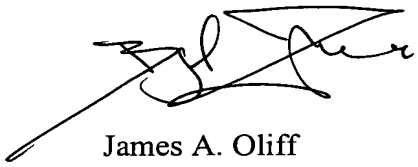
In accordance with the above remarks, Applicant respectfully submits that claim 1 defines patentable subject matter. Claims 2 and 4 depend from claim 1, and therefore, also define patentable subject matter. Accordingly, Applicant respectfully requests that the Examiner withdraw the §102(b) and §103(a) rejections.

Further, Applicant respectfully solicits rejoinder of claims 18-20.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-2, 4, and 18-20 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Bogdan A. Zinchenko
Registration No. 57,473

JAO:BAZ/hs

Date: August 7, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461